AS5001 Low Jitter Differential Silicon Oscillator

Description

The AS5001 Arcadium™ all-silicon oscillator utilizes proprietary frequency synthesis and sensor technologies to provide a quartz-free, MEMS-free, low jitter clock at any output frequency. The device is factory-programmed to output frequencies ranging from 10 kHz to 350 MHz with 0.026 ppb resolution and maintains low jitter across its operating range. The AS5001 uses on-chip temperature and strain sensors, and an advanced LC tank architecture to achieve excellent reliabilities even in high impact shock scenarios.

AS5001's on-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low jitter clocks in noisy systems that use switched- mode power supplies. Offered in a variety of industry-standard packages, the AS5001 has a dramatically simplified supply chain that enables Aeonsemi to ship samples shortly after receipt of order. The AS5001 is factoryconfigurable for a wide variety of user specifications, including frequency, output format,
with oscillatoes.-5193(Tins)-36p-prcesnsag-

1. Ordering Guide

XO Series	Description
5001	Fixed Frequency

	Device Type
A	General

	Package
A	5032
B	3225

A	Temperature Grade
I	-40 to 85 °C

Signal Format	VDD Range	Code
LVPECL (Standard)	2.5, 3.3 V	A
LVPECL (Self-Biased)	2.5, 3.3 V	B
LVDS	1.8 V	C
LVDS	2.5, 3.3 V	
CML	1.8, 2.5, 3.3 V	E
HCSL (50ohm Termination)	1.8, 2.5, 3.3 V	
HCSL (42.5ohm Termination)	1.8, 2.5, 3.3 V	G
	1.8, 2.5, 3.3 V	

Frequency Code	Description
Mxxxxxxx	FCLK < 1 MHz
xMxxxxxx	1 MHz <= FCLK < 10 MHz
xxMxxxxx	10 MHz <= FCLK < 100 MHz
xxxMxxxx	100 MHz <= FCLK <= 350 MHz

Device Revision

Note:

2. Electrical Specifications

Table 2.1. Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Temperature Range						
Temperature Range	T_A	-40	—	85	°C	Industrial grade
		-40	—	105	°C	Extended industrial grade
Supply Voltage and Power Consumption						
Supply Voltage	V_{DD}	1.71	—	3.47	V	
Supply Current (F_{CLK} = 156.25 MHz)	I_{DD}	—	40	50	mA	Tristate Hi-Z (OE = 0)
		—	1	2	mA	Ready State (ACT = 0)
		—	70	80	mA	LVPECL (Standard)
		—	60	70	mA	LVPECL (Self-Biased)
		—	45	55	mA	LVDS
		—	60	70	mA	HCSL
		—	60	70	mA	CML
		—	40	55	mA	Single LVCMOS (C_L = 15 pF)
		—	60	70	mA	Dual LVCMOS (C_L = 15 pF)
Frequency Range						
Frequency Range	F_{CLK}	0.01	—	212.5	MHz	LVCMOS output
		0.01	—	350	MHz	Differential output
Frequency Tolerance						
Initial frequency accuracy	F_{INIT}	-10	—	10	ppm	Inclusive of initial frequency tolerance at 25°C and variations over supply voltage, load and humidity after soldering-reflow shift settles.
Temperature stability	F_{STAB}	-20	—	20	ppm	-20 - 85°C
		-35	—	35	ppm	-40 - 85°C
		-35	—	35	ppm	-40 - 105°C
Aging	F_{AGING}	-5	—	5	ppm	10 Year at 25 °C
IO Characteristics						
Output enable (OE)	V_{IH}	0.7×V_{DD}	—	—	V	Input high voltage
	V_{IL}	—	—	0.3×V_{DD}	V	Input low voltage
	R_{PUP}	—	50	—	kΩ	Internal pull-up resistor to V_{DD}
	T_D	—	—	3	us	Output disable time, F_{CLK} >10 MHz
	T_E	—	—	20	us	Output enable time, F_{CLK} >10 MHz
Device active (ACT)	V_{IH}	0.7×V_{DD}	—	—	V	Input high voltage
	V_{IL}	—	—	0.3×V_{DD}	V	Input low voltage
	R_{PUP}	—	50	—	kΩ	Internal pull-up resistor to V_{DD}
	T_D	—	—	3	us	Output disable time, F_{CLK} >10 MHz
	T_S	—	—	40	us	Device standby time, F_{CLK} >10 MHz
	T_E	—	—	400	us	Device enable time, F_{CLK} >10 MHz

Continued on next page

Table 2.2. PCIe Clock Output Performance (100MHz HCSL)

Parameter	Specification	Max	Unit	Test Condition
PCIe Gen 1.1	N/A	0.311	ps	Includes PLL BW 1.5 - 22 MHz Peaking = 3dB, T_D=10 ns
PCIe Gen 2.1	3.1	0.022	ps	Includes PLL BW 5MHz & 8 - 16 MHz Peaking = 0.01 - 1 dB & 3 dB, T_D=12ns Low Band, F < 1.5 MHz
	3.0	0.259	ps	Includes PLL BW 5MHz & 8 - 16 MHz Peaking = 0.01 - 1 dB & 3 dB, T_D=12ns High Band, 1.5 MHz < F < Nyquist
PCIe Gen 3.0 common clock	1	0.085	ps	Includes PLL BW 2 - 4 MHz & 5 MHz Peaking = 0.01 - 2dB & 1dB, T_D=12 ns CDR = 10 MHz
PCIe Gen 4.0 common clock	0.5	0.085	ps	Includes PLL BW 2 - 4 MHz & 5 MHz Peaking = 0.01 - 2dB & 1dB, T_D=12 ns CDR = 10 MHz
PCIe Gen 5.0 common clock	0.15	0.033	ps	Includes PLL BW 500 kHz - 1.8 MHz Peaking = 0.01 – 2dB, T_D=12 ns CDR = 20 MHz
PCIe Gen 6.0 common clock	0.1	0.021	ps	Includes PLL BW 500 kHz – 1 MHz Peaking = 0.01 – 2dB, T_D=12 ns CDR = 10 MHz

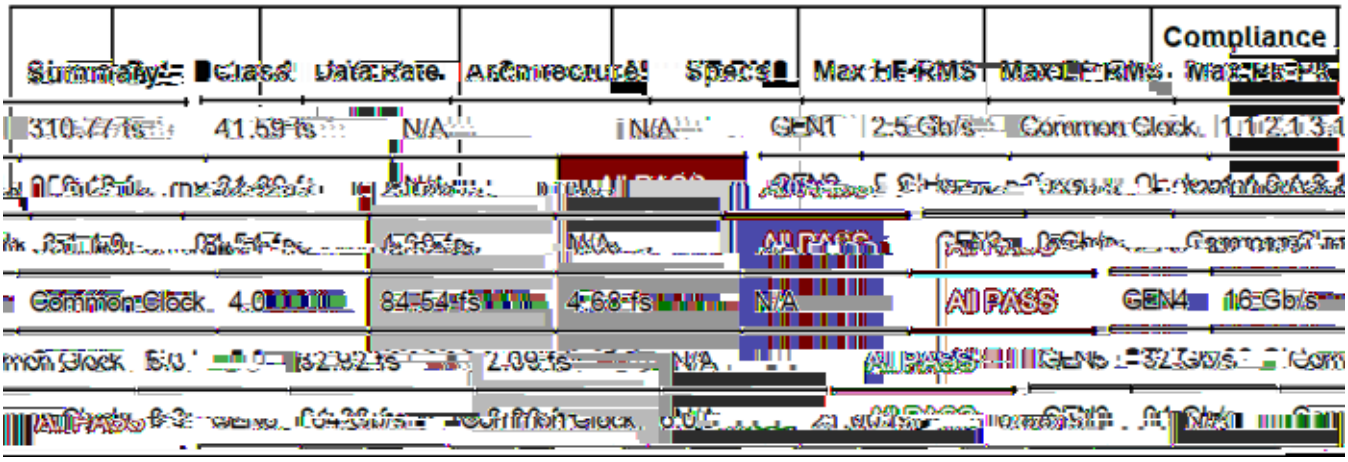


Figure 2.1. PCI-Express clock Compliance Summary

Table 2.3. Environmental Compliance and Package Information

Parameter	Value
Moisture sensitivity level (MSL)	1

Notes:

For additional product information not listed in the data sheet (e.g. RoHS Certifications, MSDS data, qualification data, REACH Declarations, ECCN codes, etc.), contact aeonsemi.com/contact_us

Table 2.4. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Maximum operating temperature	T_{AMAX}	125	°C
Storage temperature	T_S	-55 - 125	°C
Supply voltage	V_{DD_MAX}	-0.5 - 3.8	V
Input voltage	V_{IN_MAX}	-0.5 - V_{DD}+0.3	V
ESD HBM (JESD22-A114)	HBM	4.0	kV
ESD CDM (JESD22-C101)	CDM	1.0	kV
Solder Temperature[2]	T_{PEAK}	260	°C
Solder time at T_{PEAK}[2]	T_P	20 - 40	sec

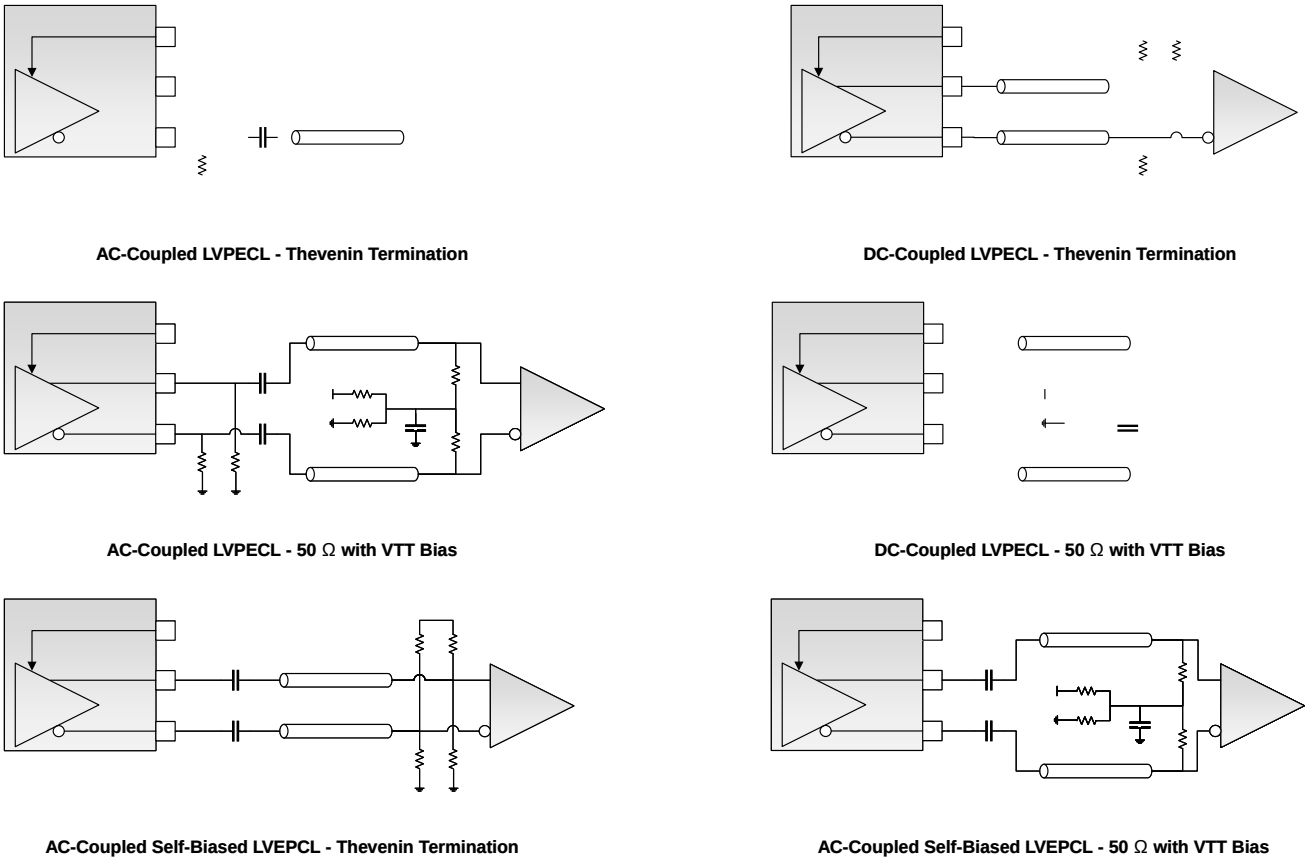
Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

3. Recommended Output Terminations

3.1. Differential Output

The output drivers support AC-coupled or DC-coupled terminations as shown in figures below.



AC-Coupled LVPECL - Thevenin Termination

DC-Coupled LVPECL - Thevenin Termination

AC-Coupled LVPECL - 50 Ω with VTT Bias

DC-Coupled LVPECL - 50 Ω with VTT Bias

AC-Coupled Self-Biased LVEPCL - Thevenin Termination

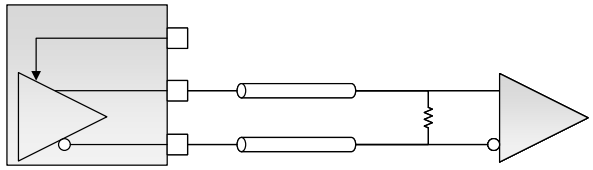
AC-Coupled Self-Biased LVEPCL - 50 Ω with VTT Bias

Figure 3.1. LVPECL Output Terminations

Table 3.1. LVPECL Termination Resistor Values

AC Coupled LVPECL Termination Resistor Values			
V_{DD}(V)	R_P	R_1	R_P
3.3 V	158 Ω	127 Ω	82.5 Ω
2.5 V	92 Ω	250 Ω	62.5 Ω

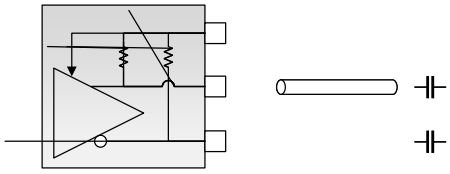
DC Coupled LVPECL Termination Resistor Values		
V_{DD}(V)	R_1	R_2
3.3 V	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω

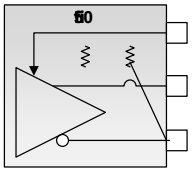


AC-Coupled LVDS

DC-Coupled LVDS

Figure 3.2. LVDS Output Terminations

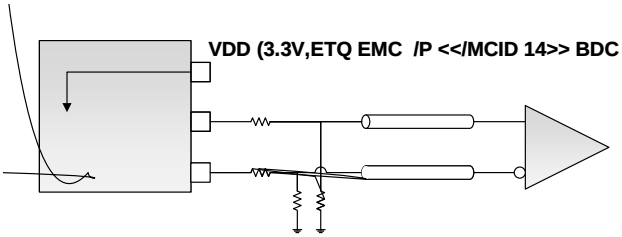


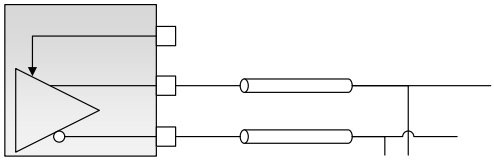


AC-Coupled CML without VCM

AC-Coupled CML with VCM

Figure 3.3. CML Output Terminations





Source Terminated HCSL

Destination Terminated HCSL

Figure 3.4. HCSL Output Terminations

3.2. CMOS Output

Dual CMOS output format options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple XOs with a single AS5001 device.



Figure 3.5. Integrated 1:2 CMOS Buffer Supports In-Phase or Complementary Outputs

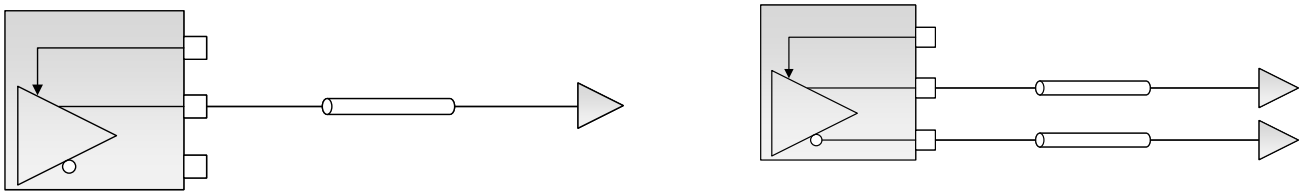


Figure 3.6. LVCMOS Output Terminations

4. Package Outline Drawing

Figure 4.1. shows the package outline drawing for the AS5001 devices. Details of dimension for different size options are listed in Table 4.1.

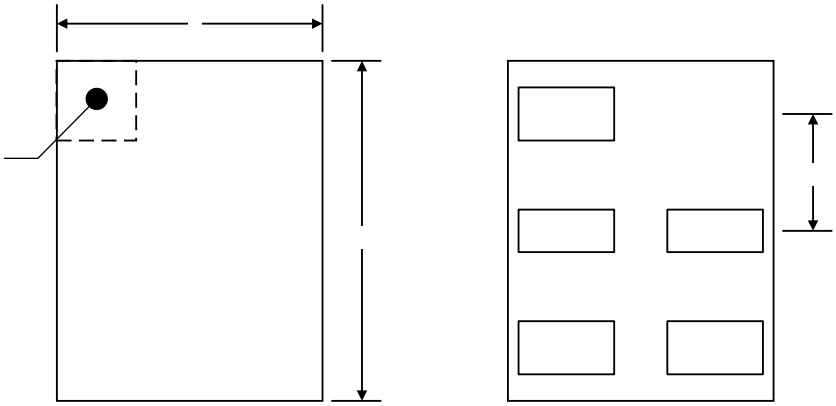


Figure 4.1. Package Outline Drawing

Table 4.1. Dimensions of Package Outline Drawing (mm)

Symbol	5032 Package	3225 Package
A	0.85 ± 0.05	0.85 ± 0.05
b	0.64 ± 0.05	0.65 ± 0.05
b1	0.64 ± 0.05	0.50 ± 0.05
D	3.20 ± 0.10	2.50 ± 0.10
e	1.27 BSC	1.175 BSC
E	4.00 ± 0.10	3.20 ± 0.10

5. Recommended PCB Land Pattern

Figure 5.1.

6. Top Mark

Figure 6.1. shows the top mark specifications for the AS5001 devices. Description of each line is listed in Table 6.1.

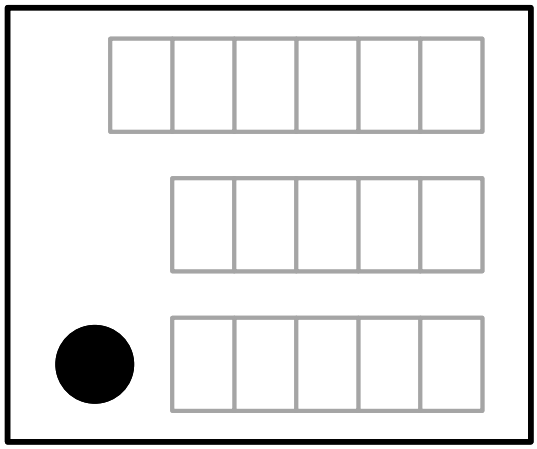


Figure 6.1. Top Mark

Table 6.1. Top Mark Description

Line	Position	Description
1	1-6	Device Name
2	1-5	Unique 5-digit Device Configuration Number
3	1	Pin 1 orientation mark (dot)
	2-3	Year (last two digits of the year), to be assigned by assembly site (ex: 2025 = 25)
	4-5	Calendar Work Week number (1-53), to be assigned by assembly site
	6	Manufacturer code

7. Packing Specification

Figure 7.1. shows the packing specifications for the AS5001 devices. Details of the tape specifications are listed in Table 7.1.

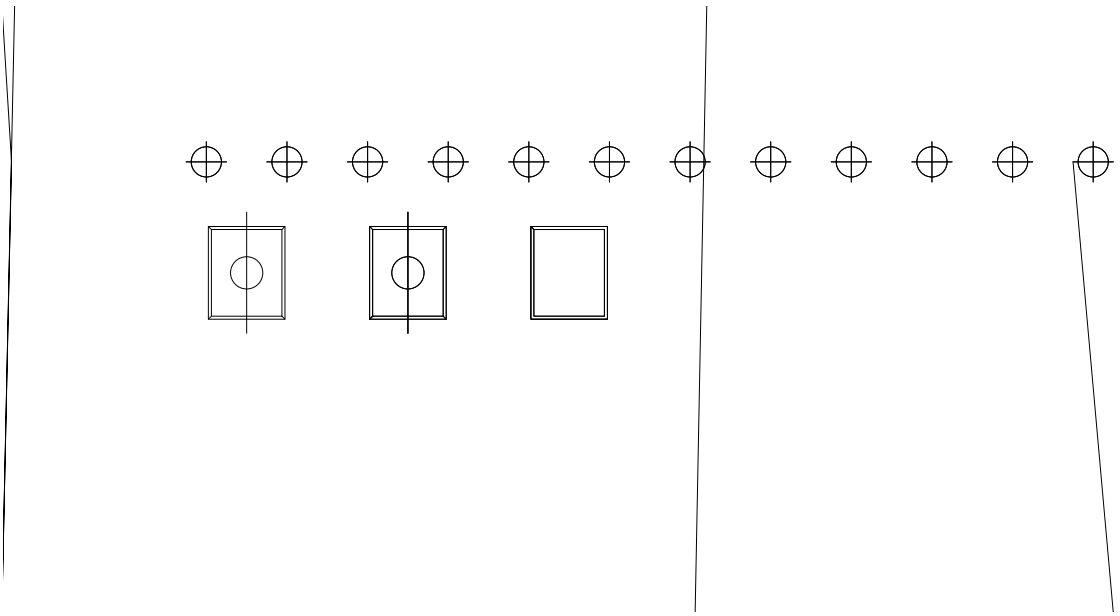


Figure 7.1. Tape Specification

Table 7.1. Dimensions of Tape (mm)

Symbol	5032 Package	3225 Package
A0	3.50 ± 0.10	2.80 ± 0.10
B0	4.30 ± 0.10	3.50 ± 0.10
K0	1.25 ± 0.10	1.05 ± 0.10
E1	1.75 ± 0.10	1.75 ± 0.10
F	5.50 ± 0.05	5.50 ± 0.05
W	12.00 ± 0.30	12.00 ± 0.30
T	0.30 ± 0.05	0.30 ± 0.05
P0	4.00 ± 0.10	4.00 ± 0.10
P1	8.00 ± 0.10	8.00 ± 0.10
P2	2.00 ± 0.05	2.00 ± 0.05
ØD0	1.50 ± 0.10	1.50 ± 0.10
ØD1	1.60 ± 0.10	1.60 ± 0.10

8. Important Notice and Disclaimer

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9. Revision History

Revision	Date	Description
1.13	Aug 2025	Corrected the tape specification
1.12	Aug 2024	Add packing specification
1.11	Mar 2024	Updated the frequency offset
1.10	Jul 2022	Updated the top mark specification
1.01	Dec 2021	Adjusted the PCB land pattern dimensions
1.00	Sep 2021	With certain specification update
0.95	Jun 2021	Corrected the Ordering Guide Insert -40 - 105 °C temperature range option Insert section “IMPORTANT NOTICE AND DISCLAIMER”
0.20	Mar 2021	Changed the frequency range and ordering guide
0.10	Feb 2021	Initial release